An Integrated CMOS Distributed Amplifier Utilizing Packaging Inductance

Patrick J. Sullivan, Bernard A. Xavier, *Member, IEEE,* and Walter H. Ku

***Abstract*— An integrated CMOS distributed amplifier is presented. The required inductance needed for the distributed waveguide structure is realized by the parasitic packaging inductance of a plastic surface-mount package. A fully packaged three-stage distributed amplifier fabricated in a 0.8-μm CMOS process is presented. The distributed amplifier has a unity gain cutoff frequency of 4.7 GHz, a gain of 5 dB, with a gain flatness of $\pm$ 1.2 dB over the 300-kHz to 3-GHz band. At a frequency of 2 GHz the amplifier has an input referred third-order intercept point of $+15$ dBm and an input referred 1-dB compression point of $+7$ dBm. The amplifier consumes 18 mA from a 3.0-V supply. The distributed amplifier is matched to 50 Ω at the input and output and has a maximum input voltage standing-wave ratio (VSWR) of 1.7:1, and a maximum output VSWR of 1.3:1 over the 300 kHz to 3 GHz band. The amplifier has a noise figure of 5.1 dB at 2 GHz.**

***Index Terms*— CMOS integrated circuits, distributed amplifiers, microwave FET amplifiers, MOSFET amplifiers, packaging, waveguide components.**

I. Introduction

PACKAGING and substrate effects can limit RF/microwave performance of silicon integrated circuits. A distributed amplifier incorporates the input and output capacitance of active devices into an artificial transmission-line structure. Similarly, packaging parasitics can be absorbed into the artificial transmission-line structure to enhance the amplifiers performance. A plastic packaged distributed amplifier is designed, which absorbs both the parasitic inductance of the package and the capacitance of active devices to form an artificial transmission line. The primary advantage of a distributed amplifier is that in absorbing the input and output capacitance's into a transmission-line structure, the gain of individual amplification stages can be added together without a corresponding decrease in bandwidth. The distributed amplifier is a well-known monolithic-microwave integrated-circuit (MMIC) design technique. It is used to realize very wide-bandwidth constant-gain amplifiers, and was first implemented over 60 years ago in vacuum tube technology [1], [2]. Most distributed amplifiers since the early 1980's have been realized as MMIC's on compound semiconductor technology (GaAs or InP).

The ideal active device for distributed amplification is a component that has a predominantly capacitive input impedance. The input impedance of a MOSFET gate is primarily capacitive making CMOS technology well suited for distributed amplification. The discrete MOSFET distributed amplifier was demonstrated over 20 years ago [3]. It was constructed with individual MOSFET devices and used bulky microstrip transmission lines fabricated on an alumina substrate to realize the inductive elements. The use of an alumina substrate prevented a low-cost integrated solution for the silicon distributed amplifier. The emergence of the GaAs MESFET with its higher operating frequencies and semi-insulating substrate made the early silicon MOSFET distributed amplifier redundant. GaAs technology could realize a fully integrated high-frequency distributed amplifier. Recently, interest in MOSFET distributed amplifiers [4], [5] has been fueled by the fact that a standard submicron CMOS process can reach operating speeds well into the microwave range [6]. However, there is still a considerable obstacle in the realization of useful CMOS distributed amplifiers due to the difficulty in realizing high-quality factor inductors and transmission lines in a standard CMOS process.

The reduced cost of CMOS integrated-circuit (IC) fabrication as compared to GaAs IC fabrication, and the reduced cost of plastic packaging as compared to ceramic packaging makes a plastic packaged CMOS distributed amplifier attractive for low-cost broad-band amplifiers operating in the low gigahertz region. Potential applications where a low-pass broad-band amplifier is required include television receivers and cable modems. Present cable-television receivers (CATV) require constant gain across the 50–850-MHz region and require very high input intercept points because over 100 channels can be incident on the receiver with no front-end filtering. Future CATV systems will likely require even larger bandwidth. A CMOS distributed amplifier would have constant gain and the high intercept point needed for such applications. The ultimate goal would be the integration of a CMOS RF front-end, together with the CMOS baseband to achieve a single-chip solution.

This paper describes a three-stage distributed amplifier. The devices are fabricated in a standard CMOS process. The silicon die is mounted in a plastic surface-mount package. The inductance of the artificial transmission line is realized by the package parasitic inductance. The resultant circuit is an integrated CMOS distributed amplifier.

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P. J. Sullivan and W. H. Ku are with the Department of Electrical and Computer Engineering, University of California at San Diego, CA 92093-0408 USA.

B. A. Xavier is with Hughes Network Systems, San Diego, CA 92121 USA.

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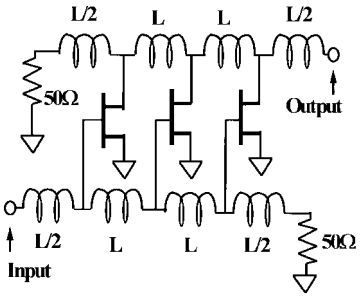


Fig. 1. Ideal three-stage distributed amplifier.

II. Implementation of Inductors, Monolithic, or Parasitic Packaging Inductor

A distributed amplifier requires two artificial transmission-line structures. The capacitance of the active devices, together with the gate and drain inductors, form a set of cascaded low-pass filter sections which act like two artificial waveguide transmission lines [15]. An ideal three-stage distributed amplifier is displayed in Fig. 1. The inductors that are needed for a distributed amplifier can be realized in two possible ways, as monolithic inductors or using the parasitic packaging inductance in the IC package.

The major concerns with monolithic inductors implemented on a silicon process are the series resistance of the interconnects and the lossy silicon substrate. Silicon processing typically uses aluminum interconnects, which have higher resistivity than the gold metallization used in GaAs processing. Silicon interconnects are typically only 1 μm thick due to the dry-etching process used, as compared to GaAs interconnects which can be several microns thick in some GaAs processes, due to the lift-off process employed. Overall, the series resistance of silicon interconnections is much higher than GaAs interconnections which degrades the quality factor (Q) of silicon inductors. Nguyen and Meyer [7] have shown that spiral inductors implemented on a standard silicon process can provide Q's of five at 1 GHz and Q's of three at 2 GHz, limited mainly by the interconnect series resistance. Recently there have been many exotic attempts to improve the Q factor of spiral inductors fabricated on silicon substrate. The techniques usually require additional process steps and depart from standard commercial silicon processing. The techniques can be divided into two categories, reduction of series loss in the inductor or reduction of losses in the substrate. In the first category, researchers have tried to reduce the inductor's series loss through gold metallization [8] or the use of multimetal layers [9]. Second category methods have tried to reduce the losses of the substrate through high-resistivity silicon substrates [10], thick oxide/polyimide deposition [11], or etching to create trench isolated inductors [12]. Even with these process modifications, it is rare to see inductors realized on a silicon substrate with peak Q factors above ten.

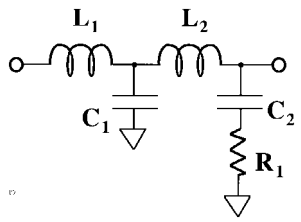
Modern plastic surface-mount packages have parasitic inductance on the order of 3 nH and these inductance's have Q factors on the order of 30 in the low gigahertz region [13]. Clearly, package inductors have significantly better quality factors than the best monolithic inductors implemented on silicon. Although packaging inductors are fixed values, which can be a design disadvantage, the most common criticism of exploiting package parasitic inductors is the repeatability of the inductance value. The main source of error is due to the variance of the bond-wire length, which depends on where the silicon die is seated in the package cavity. Inductors implemented with packaging inductance require extra packaging pin's and the only active die area required is the bond pad. Monolithic inductors occupy considerable active die area and realize lower Q's. The real cost of exploiting package parasitics is the expense of using additional package pin's to realize the artificial transmission lines. If there are spare package pin's, then a package inductance distributed amplifier is feasible. If a larger package is required, a more economical solution should be sought.

III. Parasitics and Passive Elements Modeling

As the frequency of silicon IC's increases into the microwave region of operation, parasitics become a significant part of the circuit. Important packaging parasitics are the bonding pads on the silicon substrate, the bonding wire, and the lead-frame inductance. These package parasitics are usually considered undesirable, but a distributed amplifier incorporates these parasitics into the artificial transmission-line structure to enhance the amplifiers performance. Lumped-element models of the bonding pad, plastic surface-mount package, and on the chip monolithic inductor were determined by extraction and optimization of two-port S-parameter measurements. There was no attempt to model substrate coupling effects on the silicon substrate.

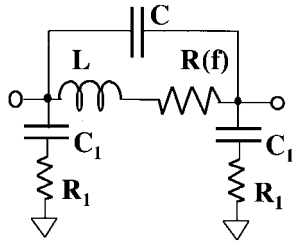
The bonding pad [90 μm $\times$ 90 μm of top layer metal ($M2$)] is modeled by a lumped-element circuit [14] consisting of a shunt parasitic capacitance and series substrate resistance. A lumped-element model of a 24-pin small shrink outline (SSOP-24) plastic surface-mount package was generated. An individual pin model is composed of a package lead and bond wire modeled by two separate series inductors and a shunt capacitor. The complete package and bonding pad lumped-element model of a single package pin is displayed in Fig. 2. Plastic packages have considerable mutual coupling between neighboring pin's at RF and microwave frequencies. The mutual inductance of the package pin's were simulated with the aid of an electromagnetic simulator. The mutual and self inductance were modeled with an inductance matrix. The finite Q factor of the package was modeled by including a small series resistance.

To assess the performance of a monolithic inductor a two-layer metal on-chip square–spiral inductor was fabricated. The inductor was a four-turn square spiral. The metal width was 18 μm with 8 μm spacing between turns. The CMOS process was a low resistivity interconnect process, which has slightly thicker metallization than a typical CMOS process. The process consisted of a 2.1-μm-thick top-layer aluminum metallization ($M2$), and a 1.1-μm-thick first-layer metal ($M1$). Top layer metal ($M2$) was separated from $M1$ by a 1.1-μm oxide (SiO_2) and $M1$ was 1.5 μm above the 10–12-Ωcm p^+ substrate. To reduce the inductor's series resistance $M2$–$M1$



Parameter	Value	Description
L_1	2.5 nH	Lead Frame Inductance
L_2	1 nH	Bond Wire Inductance
C_1	300 fF	Lead Frame Package Capacitance
C_2	53 fF	90 x 90 μm^2 Bond Pad Capacitance
R_1	160 Ω	90 x 90 μm^2 Bond Pad Substrate Resistance
K_1	0.3	Inductor Coupling Coefficient, Nearest Neighbor
K_2	0.1	Inductor Coupling Coefficient, Next-nearest Neighbor

Fig. 2. Lumped-element model of a packaging pin.



Parameter	Value	Description
L	2.4 nH	Inductance
R(f)	3.5 Ω	Series Resistance
C	14 fF	Capacitance between Inductor Windings
C_1	.672 pF	Capacitance to the Substrate
R_1	334 Ω	Substrate Resistance
K_1	0.6	Frequency Dependent Fitting Constant
K_2	1.3	Frequency Dependent Fitting Constant

Fig. 3. Lumped-element model of a monolithic inductor. Two-layer metal CMOS process.

vias were place along the entire length of the square–spiral inductor. The on-chip square–spiral inductor was modeled as a lumped element with a frequency-dependent resistor. The frequency-dependent resistor models the dc series resistance and the nonuniform current flow in the inductor at high frequencies due to the skin effect. The frequency-dependent resistor is modeled [8] as $R_S = R_0(1 + K_1 f^{K_2})$, where R_0 is the dc series resistance, f is the frequency in gigahertz, and K_1 and K_2 are curve-fitting constants. Two-port S-parameter measurements were conducted on the monolithic inductor with both ports floating. A lumped-element model was derived in Fig. 3. The capacitor in parallel with the inductor represents the capacitance between the turns. The parasitic capacitance to the substrate, and substrate loss, is modeled with a capacitor in series with the resistor connected to ground.

IV. Active-Device Modeling

CMOS foundries invest significant effort in device modeling, but the models are primarily intended for digital CMOS design at baseband frequencies. Typically, CMOS foundries supply the designer with a BSIM (Berkeley Short Channel IGFET) SPICE model. The accuracy of the foundry supplied BSIM SPICE models at microwave frequencies is questionable since the capacitance values are generally determined by dc extraction and verified against propagation delay measurements. An inverter or chain of inverters is used to measure the propagation delay. Clearly, the CMOS devices are transitioning between cutoff and the ohmic region when the propagation delay is measured. Microwave circuits generally require the active devices to be operated in the saturation region, with the exception of some power-amplifier applications. An additional area of concern is the fact that the BSIM-II SPICE model does not account for gate resistance. This is an important parameter in noise-figure computations and high-frequencies performance. As was noted in early GaAs MESFET distributed amplifiers [15], gate resistance causes gain rolloff at high frequencies. The gate material used in CMOS technology is either silicided polysilicon or nonsilicided polysilicon. With present standard CMOS processing (silicided polysilicon sheet resistance is on the order of 4 Ω/□), nonsilicided polysilicon is significantly higher on the order of 90 Ω/□. The total gate

resistance is a layout-dependent parameter and can be lowered by practices such as multifinger transistors and gate contacts with multiple vias on both sides of the polysilicon gate.

V. Review of the Theoretical Gain and Theoretical Noise Figure

Aitchison [16] and Beyer *et al.* [17] have shown for an idealized loss-free distributed amplifier that the small signal gain G is predicted by (1), where g_m is the transconductance of each stage in the distributed amplifier and N is the number of stages of the distributed amplifier. A further simplification is valid when two conditions hold. First, if the gate-line phase constant β_g and drain-line phase constant β_d are equal, then the gain becomes independent of frequency and is maximized. Secondly, if the characteristic impedance of the gate-line $Z_{\pi g}$ and drain-line $Z_{\pi d}$ become equal to the characteristic impedance Z_0, then (2) is valid. In theory, there is no restriction on the gain-bandwidth product. The gain can be theoretically increased indefinitely by increasing the number of stages N, while the bandwidth remains constant. This only applies for the loss-free case. In order to approximate this ideal case, the inductors used to realize the artificial transmission line should have as high a Q factor as is possible:

$$G = \frac{g_m^2 Z_{\pi g} Z_{\pi d}}{4}\left(\frac{\sin\frac{N}{2}(\beta_g-\beta_d)}{\sin\frac{1}{2}(\beta_g-\beta_d)}\right)^2 \tag{1}$$

$$G = \left(\frac{N g_m Z_0}{2}\right)^2. \tag{2}$$

Van der Ziel [18]–[20] has postulated that only two noise sources are present in an FET, a channel thermal-noise source $\overline{i_d^2}$, and a gate thermal-noise source $\overline{i_g^2}$. These noise sources can also be correlated, which can be modeled with a complex correlation coefficient:

$$\overline{i_d i_d^*} = \gamma 4kTg_{d0}\Delta f \qquad \overline{i_g i_g^*} = \delta 4kTg_g\Delta f,$$
$$\text{where} \quad g_g = \frac{w^2 C_{\rm gs}^2}{5g_{d0}}. \tag{3}$$

In the above thermal-noise sources g_{d0} is the zero-bias drain conductance, γ is the drain noise coefficient, δ is the gate noise coefficient, and g_g is the induced gate conductance. The drain noise coefficient γ is a bias-dependent parameter, but is typically between $2/3 < \gamma < 1$ for long-channel MOSFET devices. For short-channel MOSFET devices operating in the saturated region, γ can be greater than one and may be as high as two or three [21]. The gate noise coefficient δ is typically $\delta = 4/3$ for long-channel MOSFET devices. For short-channel MOSFET devices, one expects δ to be larger due to hot electron effects. Aitchison [16] analyzed the noise figure of a GaAs MESFET distributed amplifier using the Van der Ziel noise model. The resulting analysis showed the noise figure decreasing with an increasing number of stages. The noise figure was shown to be approximated by (4) for a large number of stages N:

$$F = 1 + \frac{Z_0 N\omega^2 C_{\rm gs}^2\delta}{3g_m} + \frac{4\gamma}{N g_m Z_0}. \tag{4}$$

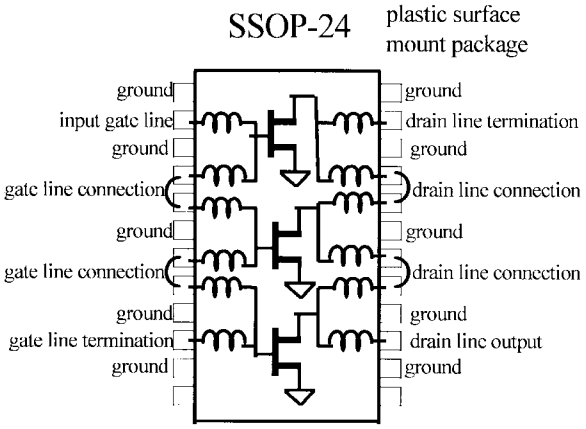


Fig. 4. Distributed amplifier utilizing packaging inductance.

Presently there is a lack of published experimental data for short-channel MOSFET drain (γ) and gate (δ) noise coefficients, although there has been recent interest in these coefficients for the design of CMOS low-noise amplifier (LNA's) for RF applications [22].

VI. Design of a CMOS Distributed Amplifier

In designing a distributed amplifier, the first step is the design of the waveguide structure. Selecting the L and C values for the waveguide sets both the characteristic impedance of the transmission line and the cutoff frequency of the waveguide. When using packaging inductance, the L component is predetermined by the selection of the package. A single-package pin is required to implement the $L/2$ inductor section. A full L inductor section is then formed from two pin's in series; the signal leaves the chip on one pin then reenters the chip on the other pin (see Fig. 4). For the SSOP-24 package that was used, a single pin which is equal to $L/2$ is 3 nH. The design choice is the size of the active device, which together with parasitics, sets the C component of the waveguide structure. With L and C values determined, the transmission-line equation determines the waveguide cutoff frequency. For example, the cutoff frequency of the gate transmission line $f_{c,\rm gate}$ is determined by the gate-line inductance L_g (fixed bond wire), and the gate-line capacitance, which is composed of active device capacitance $C_{\rm GS}$ (design choice) and the parasitic capacitance C_p, as represented by (5). The units in the transmission-line equation are in inductance or capacitance per unit length or can be viewed as inductance or capacitance per section of the distributed amplifier as follows:

$$f_{C,\rm gate} = \frac{1}{2\pi\sqrt{L_B(C_{\rm GS}+C_P)}}. \tag{5}$$

We are also interested in the drain-line capacitances. Typically, when designing distributed amplifiers on GaAs extra capacitance, C_1 is added to the drain line to ensure $C_{\rm GS} = C_{\rm DS} + C_1$, which aids in keeping a constant phase relationship between the input and output signals. The CMOS distributed amplifier has a extra capacitance on the drain line, the drain-bulk capacitance $C_{\rm DB}$, which a GaAs distributed amplifier does not have due to the insulating substrate. The MOSFET

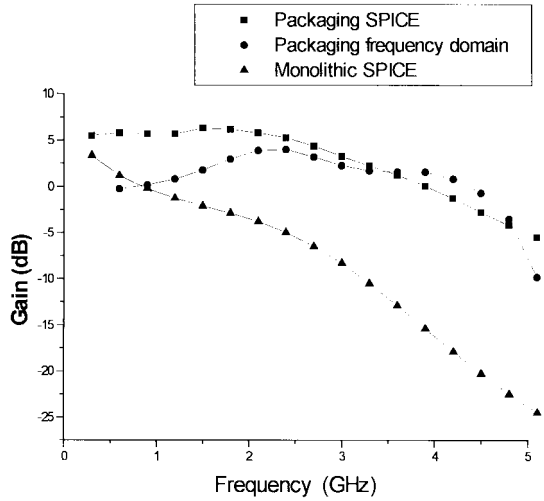


Fig. 5. Initial simulated $|S_{21}|^2$ implementations for monolithic inductors and packaging inductors.

drain capacitance is due to both drain-body capacitance $C_{\rm DB}$ and drain-source capacitance $C_{\rm DS}$ of the active device. The drain was design larger than normal to increase the drain-line capacitance via an increase of $C_{\rm DB}$, which aided in phase matching the two transmission lines.

VII. Simulation of a CMOS Distributed Amplifier

The derived lumped-element models were used in conjunction with MOSFET device models to design and predict the performance of a three-stage distributed amplifier in both a time-domain circuit simulator and frequency-domain circuit simulators.

To evaluate the performance of the monolithic distributed amplifier as compared to a package inductance distributed amplifier, S-parameter simulations were undertaken. Two-port S-parameters were simulated using the linear analysis capabilities of a time-domain simulator (SPICE) and the small-signal frequency-domain simulator of a harmonic-balance tool for comparison. The time-domain simulator utilized modified BSIM-I SPICE models (implemented as HSPICE level $= 28$), whereas the frequency-domain simulator employed level-three MOS models. Fig. 5 shows a comparison of $|S_{21}|^2$ of the two distributed amplifiers at the bias conditions of 18.0 mA from a 3.0-V supply. This bias point was used for all simulations and measurements. The distributed amplifier realized with monolithic inductors has a very poor gain ($|S_{21}|^2 = -4$ dB at 2 GHz) when compared to the amplifier utilizing package inductance ($|S_{21}|^2 = 5$ dB at 2 GHz). The additional loss arises due to the low Q factor of the monolithic inductors. Typical uses of spiral inductors in silicon RF IC's are as RF loads or degereration inductors—rarely does the signal path transverse across the entire inductor. When the spiral inductor is in series with the signal path, insertion loss becomes a critical factor. The insertion losses due to the spiral inductors are accumulative in a distributed amplifier topology and have a direct effect on the gain and noise figure of the monolithic distributed amplifier. The insertion loss of a monolithic inductor L section was simulated and determined to be 0.8 dB.

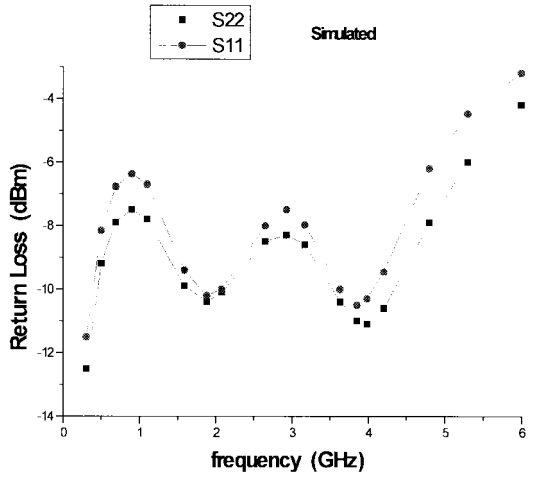


Fig. 6. Simulated $|S_{11}|$ and $|S_{22}|$.

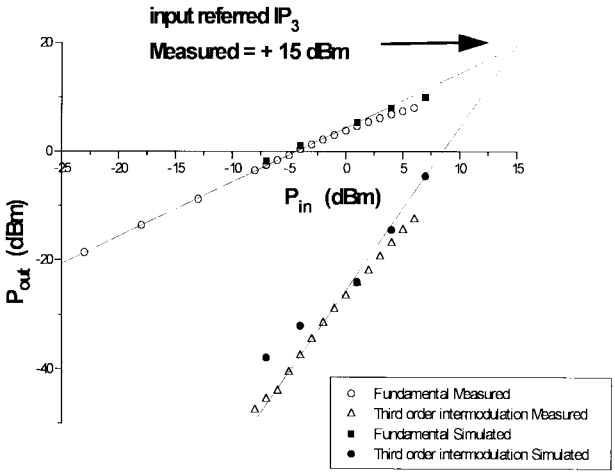


Fig. 7. Measured and simulated input referred third-order intercept point.

From the simulated results there seems very little advantage in implementing a distributed amplifier using spiral inductors with present interconnection technology.

Further simulations were conducted for the package inductance distributed amplifier with the time-domain simulator SPICE utilizing the modified BSIM-I models. The simulated reflection coefficients $|S_{11}|^2$ and $|S_{22}|^2$ are shown in Fig. 6. The third-order input–intercept point was simulated by applying two equal tones spaced 50 MHz apart; two simulations were undertaken at number of different power levels to ensure the distributed amplifier was not in compression (Fig. 7). The 1-dB compression point was simulated by sweeping the input power of a single-tone source (2 GHz) from -40 dBm to $+10$ dBm in 1-dBm steps (see Fig. 8). The noise figure of the packaging inductance distributed amplifier was simulated and is displayed in Fig. 9. A simulation of $|S_{21}|^2$ of the distributed amplifier with the lumped gate resistance varied from 20 to 100 Ω in increments of 40 Ω, shown in Fig. 10. Clearly, the gate resistance parameter has a significant effect on the gain flatness and the cutoff frequency of the amplifier. Existing SPICE models such as BSIM-I, modified BSIM-I, and BSIM-II (HSPICE level 13, 28, and 39) do not adequately model

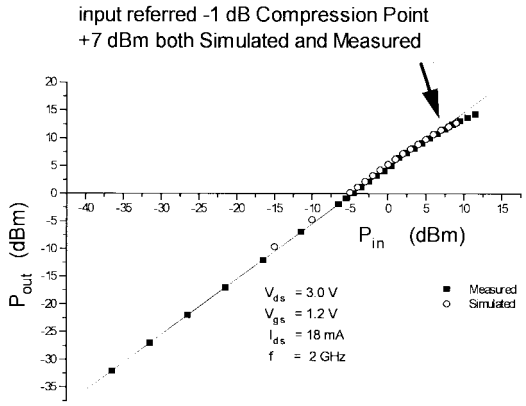


Fig. 8. Measured and simulated input referred -1-dB compression point.

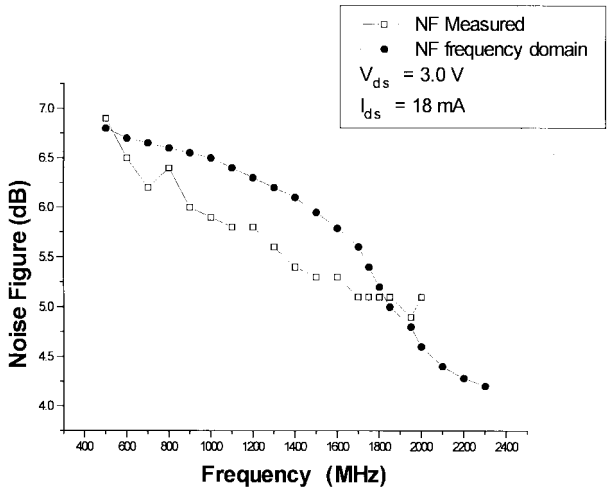


Fig. 9. Measured and simulated noise figure.

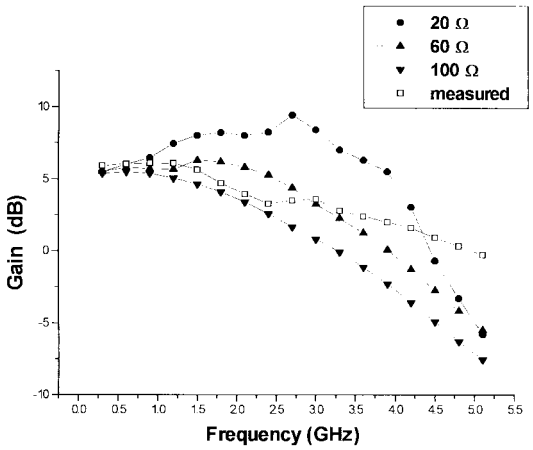


Fig. 10. Simulated $|S_{21}|^2$ for different lumped gate resistance's compared to measured $|S_{21}|^2$.

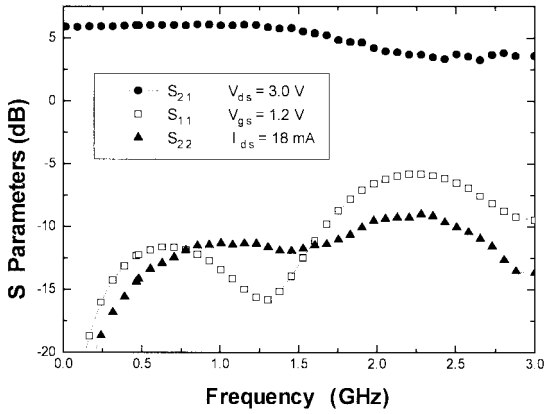


Fig. 11. Measured S-parameters.

gate resistance, and caution should be used when designing cutoff frequencies of a CMOS distributed amplifier with such models. The proposed BSIM 3v3 MOS model includes gate resistance as the modeled parameter and should help alleviate the present situation.

VIII. Experimental Results

A distributed amplifier that utilized the parasitic packaging inductance to create a waveguide structure was constructed. The distributed amplifier was fabricated on a commercial 0.8-μm CMOS n-well two-layer metal process. MOSFET gate resistance was minimized to reduce gate transmission-line loss in the distributed amplifier—a salicide process and the physical layout of multiple fingers aided in this goal. Three NMOS devices were used as the active elements in the three-stage distributed amplifier. Each active device consisted of 20-finger single-sided gate contacts, with dimensions of 20×0.8 μm per finger. This gives a total gatewidth of 400 μm. The distributed amplifier occupied an active area of 720×320 μm, including all bond pads. The distributed amplifier IC die was encapsulated inside a SSOP-24 plastic surface-mount package. To minimize ground lead inductance, three down bonds in total were utilized (one down bond per stage) from the IC to the metal package ground plane (paddle). The IC was epoxied with nonconductive epoxy to the metal paddle. The epoxy maintains good mechanical and thermal contact between the IC and the package, but no electrical contact between the backside of the silicon IC and the paddle. The ground plane (paddle) achieved a good RF ground with six lead-frame pin's, which were tied to PCB ground and physically attached to the package ground plane (paddle). The total ground lead inductance was estimated to be 0.9 nH. This technique obviates the need for a backside grounded IC, which requires additional processing steps and additional cost when compared to standard silicon IC packaging technology. The plastic surface-mount package was soldered onto a standard fiberglass printed circuit board (FR4). Two 50-Ω microstrip lines on the PCB mated the gate input line and the drain output line to two SMA connectors, which enabled two-port measurement. Bias was provided by two microwave bias-Tees.

All measurements were taken under identical dc-bias conditions: 3 V on the drain line and 1.2 V on the gate line. At this bias point the distributed amplifier consumed 18 mA, requiring a total power dissipation of 54 mW. Fig. 11 shows two-port S-parameter measurements from 300 kHz to 3 GHz. The distributed amplifier is matched to 50 Ω at the input and output and achieves a measured gain of $+5$ dB with an associated gain flatness of $+/-1.2$ dB in the 300-kHz to 3-GHz band. The maximum input voltage standing-wave ratio (VSWR) was 1.7:1 and the maximum output VSWR was 1.3:1, which

TABLE I
COMPARISON OF MEASURED, SIMULATED, AND THEORETICAL RESULTS

	MEASURED	SIMULATED	THEORETICAL
Conversion Gain	5 dB	6 dB	6.9 dB
Noise Figure	5.1 dB	5.2 dB	2.5 dB
input IP3	+15 dBm	+12.5 dBm	-
input 1 dB Compression	+7 dBm	+7 dBm	-

corresponds to $|S_{11}|^2 < -6$ dB and $|S_{22}|^2 < -9$ dB (300 KHz–3 GHz). The amplifier has a unity gain cutoff frequency of 4.7 GHz. Fig. 7 shows a two-tone IP3 measurement at 2.00 and 2.05 GHz, resulting in a measured input referred third-order intercept point of +15 dBm. Fig. 8 shows an input referred 1-dB gain compression of +7 dBm, measured at 2 GHz. At room temperature, noise-figure measurements were taken (with reference to a 50-Ω source resistance) from 500 MHz to 2 GHz (see Fig. 9), and the noise figure is 5.1 dB at 2 GHz.

Using the simulated transconductance of a single stage yields a theoretical gain of 6.9 dB. Assuming the MOSFET is operating as a ideal long channel device—a rather poor assumption—then the noise coefficients are $\gamma = 2/3$ and $\delta = 4/3$, resulting in a theoretical noise figure of 2.5 dB. Comparison between theoretical, simulated, and measured results are shown in Table I.

IX. CONCLUSION

Today's CMOS technology is capable of producing active devices operating in the RF and low microwave band. Inductors implemented monolithically on the silicon substrate with present-day interconnect and substrate technology have large high-frequency losses associated with the series resistance and the shunt capacitance to the substrate. Future improvements in submicron multilayer metal interconnects will allow the use of high Q-factor monolithic inductors and should pave the way for fully monolithic CMOS distributed amplifiers.

Using a standard commercial CMOS process and a plastic surface-mount package, an inexpensive fully packaged CMOS distributed amplifier has been demonstrated. The three-stage distributed amplifier uses a novel packaging technique to exploit packaging parasitics to realize the required inductance for distributed amplification. The distributed amplifier is fully packaged with no external components, making it the first fully integrated distributed amplifier implemented in a CMOS technology. The distributed amplifier has a unity gain cutoff frequency of 4.7 GHz, a gain of 5 dB, input referred third-order intercept point of +15 dBm, a +7 dBm input referred 1-dB compression point, and 5.1-dB noise figure at 2 GHz, while consuming 18 mA from a 3-V supply.

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Patrick J. Sullivan is currently working toward the Ph.D. degree in electrical and computer engineering at the University of California at San Diego.

His present research interests are in CMOS communication circuits for L-band applications. He has designed analog and RF integrated circuits for Pacific Communication Sciences Inc. and Rockwell Semiconductor Systems.

Bernard A. Xavier (M'90) received the first-class honors degree from Kingston Polytechnic, London, U.K., in 1989, and the Ph.D. degree from Brunel University, London, U.K., in 1992.

In 1989, he began working for Texas Instruments, U.K. He is currently working for Hughes Network Systems, San Diego, CA. He has over eight years experience in RF IC and analogue IC design. His current research interests lie in radio transceivers and associated circuitry.

Dr. Xavier received the Institution of Electrical Engineers (IEE) (U.K.) prize for distinction in 1989.

Walter H. Ku received the B.S. degree with honors from the Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, in 1957, and the M.S. and Ph.D. degrees from the Polytechnic Institute of Brooklyn, NY, in 1962.

In 1977, he was the first occupant of the Naval Electronic Systems Command (NAVELEX) Research Chair Professorship at the Naval Postgraduate School, Monterey, California. As the NAVELEX Research Chair Holder, he was an Expert Consultant to NAVELEX (now SPAWAR), Naval Research Laboratory (NRL) and OUSDRE. He has served over the years as a Consultant to DOD (DDR&E and ARPA) on the VHSIC and various GaAs monolithic integrated circuits programs, including the first DARPA-funded C- and X-band Space-Based Radar Modules, Air Force RADC, Griffith AFB, NY, and industrial laboratories. Since 1985, he has been Professor of electrical and computer engineering at the University of California at San Diego, and is the Founding Director of the NSF I/UC Research Center on Ultra-High Speed Integrated Circuits and Systems (ICAS).

Dr. Ku is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Tau, Phi Tau Phi and Sigma Xi. He is also the principal investigator of a new five-year $6 000 000 grant from DDR&E Focused Research Initiative (FRI) on Broad-Band Wireless Multimedia (BWM) Communications Systems. This FRI Program was awarded in January 1995 and is a consortium lead by UCSD with Advanced Digital Technology (ADT), Hughes, Raytheon, Rockwell, and TRW as team members.